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REMARKS

The Examiner has rejected Claims 1-25 under the judicially created doctrine of obvious-type double patenting as being unpatentable over Claims 1-3, 5-13, and 22-33 of U.S. Patent No. 6,647,456. Submitted herewith is a terminal disclaimer that renders such rejection moot.

The Examiner has further rejected Claims 1-9, 11-13, and 15-23 under 35 U.S.C. 103(a) as being unpatentable over Novak et al. (US Patent No. 6,295,586, hereinafter "Novak") in view of Kessler et al. (US Patent No. 6,622,225, hereinafter "Kessler"). Applicant respectfully disagrees with such rejection.

Specifically, the Examiner relies on the following excerpt from Kessler to make a prior art showing of applicant's claimed "wherein the memory controller is capable of restoring the activate commands to a row and a bank associated with the read or write commands at a head of a read or write queue" (see all independent claims, except Claims 24-25).

"A computer system includes a memory controller interfacing the processor to a memory system. The memory controller supports a memory system with a plurality of memory devices, with multiple memory banks in each memory device. The memory controller supports simultaneous memory accesses to different memory banks. Memory bank conflicts are avoided by examining each transaction before it is loaded in the memory transaction queue. On a first clock cycle, the new pending memory request is transferred from a pending request queue to a memory mapper. On the subsequent clock cycle, the memory mapper formats the pending memory request into separate signals identifying the DEVICE, BANK, ROW and COLUMN to be accessed by the pending transaction. In the next clock cycle, the DEVICE and BANK signals are compared with every entry in the memory transaction queue to determine if a bank conflict exists. If so, the new memory request is rejected and recycled to the pending request queue." (see Abstract)

Still yet, the Examiner argues that 'read or write memory requests that result in a bank conflict are rejected and recycled through the pending request queue which eventually makes its way down to the head of the queue to generate or "restore" the appropriate signals or commands, including those required to activate the

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appropriate rows and columns for memory access.'

Applicant respectfully disagrees with this assertion. First, there is absolutely
no mention of any sort of "activate commands" in the foregoing Abstract excerpt.
Still yet, the only suggestion of "activate commands" in Kessler is in the following
except:

> "The Control line Precharge coupled to the DRAM core transmits a
> precharge command that, along with the DEVICE and BANK address
> values, causes the selected memory bank to release its two
> associated sense amplifiers. This permits a different row in that
> memory bank to be activated or permits adjacent memory banks to be
> activated. The RowA control line coupled to the DRAM core transmits
> an Activate command that, along with the DEVICE, BANK and ROW
> address values, causes the selected row of the selected bank to be
> loaded into its associated sense amplifiers (two 512 byte sense
> amplifiers for DQA and two 512 byte sense amplifiers for DQB). The
> ColCRd command is issued with a DEVICE, BANK, and COLUMN address
> value to transfer a column of data (16 bytes) from one of the two
> sense amplifiers shared by the memory bank through the DQA/DQB data
> paths to the RAMbus.TM. interface logic. The data is then output to
> the Zbox 190 memory controller. A ColCWr command transfers a column
> of data from the Zbox memory controller 190 through the RAMbus.TM.
> interface logic and DQA/DQB data paths to one of the two sense
> amplifiers identified by the DEVICE, BANK and COLUMN address
> values." (see col. 14, lines 16-38)

Such excerpt, however, makes absolutely no disclosure, teaching, or
suggestion of "restoring the activate commands to a row and a bank associated with
the read or write commands at a head of a read or write queue." Only applicant
teaches and claims a memory controller with such restoring capability, as
specifically claimed.

It appears that the Examiner has attempted to argue that Kessler is capable,
in some hypothetical situation, to meet applicant's claim language. It further
appears that the Examiner has failed to consider the full weight of applicant's
claimed "restoring," during the course of such argument. Following is an exemplary
dictionary definition to illustrate one illustrative example of the plain and ordinary
meaning of "restoring."

> 1. To bring back into existence or use; reestablish;
> 2. To bring back to an original condition;
> 3. To put (someone) back in a former position;
> 4. To make restitution of; give back.

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Thus, from the above exemplary definition, it is clear that the mere alleged suggestion of *generating* activation commands, in no way meets applicant's claimed "restoring," let alone "restoring the activate commands to a row and a bank associated with the read or write commands at a head of a read or write queue," as claimed. Only applicant teaches and claims such a unique feature.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Applicant respectfully asserts that the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to at least suggest all of applicant's claim limitations. Again, a notice of allowance or a specific prior art showing of each of the foregoing limitations, in combination with the remaining claim elements is respectfully requested.

The Examiner has further rejected Claims 10, 24, and 25 under 35 U.S.C. 103(a) as being unpatentable over Novak in view of Kessler and further in view of Margulis (US Patent No. 6,057,862) Still yet, the Examiner rejected Claim 25 under 35 U.S.C. 102(e) as being anticipated by Margulis. Applicant respectfully disagrees with such rejections, especially in view of the amendments made hereinabove.

Specifically, the Examiner relies on the following excerpts from Margulis to meet applicant's claimed three memory controller subsystems coupled to a graphics

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unit computer component, central processing computer component, and display refresh module computer component.
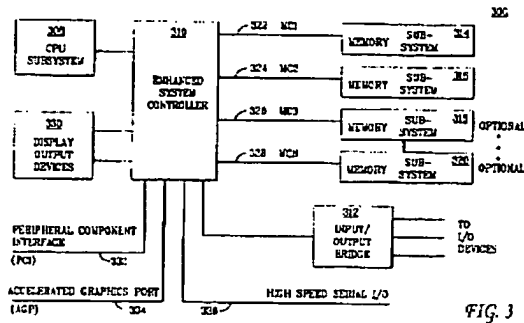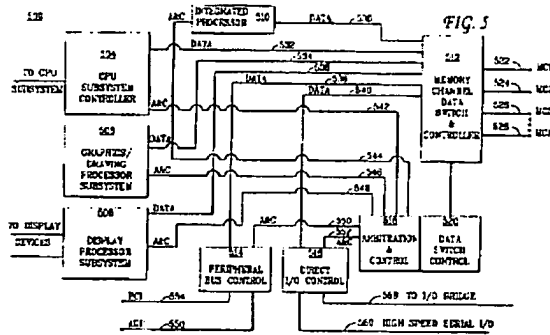

FIG. 3

FIG. 5

Applicant has amended independent Claims 24 and 25 to clearly distinguish such prior art, which clearly share memory controllers. Specifically, now claimed is "wherein a first one of the memory controller subsystems is coupled only to a graphics unit computer component. a second one of the memory controller subsystems is coupled only to a central processing computer component, and a third one of the memory controller subsystems is coupled only to a display refresh module computer component" (emphasis added). Only applicant teaches and claims that each memory subsystem coupled only to one computer component. It is believed that the Examiner alluded to this fact in his statement: "[n]ote that the claims do not require that each memory subsystem couple to only one computer component."

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that the Examiner alluded to this fact in his statement: "[n]ote that the claims do not require that each memory subsystem couple to only one computer component."

A notice of allowance or a specific prior art showing of each of the foregoing limitations, in combination with the remaining claim elements is respectfully requested.

Applicant further brings the Examiner's attention to the following new claims which include subject matter believed to be allowable:

"wherein the restoring utilizes a field in the read or write queue that contains an activate write address" (see Claim 26); and

"wherein the activate write address is indicated by a write pointer when the activate queue is written" (see Claim 27).

Again, a notice of allowance or a specific prior art showing of each of the foregoing limitations, in combination with the remaining claim elements is respectfully requested.
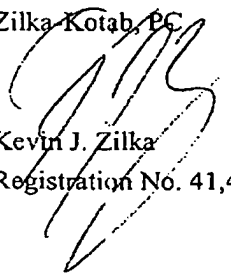
All of the independent claims are deemed allowable. Moreover, the remaining claims are also deemed allowable by virtue of their dependence from the independent claims. An allowance is respectfully requested.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. For payment of any fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP033A/P000873).

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Respectfully submitted,

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